Modeling of long-term EMC of electronic equipment in multi-stress environment

In numerous safety-critical applications (e.g. aeronautics, spatial, medical, automotive), electronic devices have to operate in harsh conditions. They are exposed continuously and simultaneously to different stress conditions such as ionizing radiation, very high or low temperature, electrical overstress, vibration, etc. These hazardous environmental conditions have a direct impact not only on integrated circuit performances, but also on electromagnetic emission and immunity, as proved in recent research works. It may compromise the overall reliability and safety of the end-user application.

In order to study and anticipate risks of EMC non compliance and related failures, an efficient method consists in developing long-term EMC models of electronic devices. These equivalent models aims at simulating the evolution of electromagnetic emission or immunity of the device according to the aging induced by the environmental conditions. The project goals are:

- explore complex ICs susceptibility to electromagnetic disturbance degradation during the lifetime and harsh environmental exposure with combined effects as in real application conditions
- propose characterization and modeling methodology to predict long-term EMC evolution at integrated circuit level. Results of previous research works will be reused and improved
- use long-term EMC model of integrated circuits for simulation at printed circuit board level to predict electromagnetic related risks of the final application according to the environmental conditions

The subject, still unexplored, requires combined stress process, optimized tests, and appropriate mathematical tools to assess the long-term reliability and EMC. The PhD student will work on the development and the validation of the fast timing test environment, design the test plan for the combined accelerated-aging stress and EMC tests, manage the EMC and high voltage/temperature tests, and develop the prediction method to determine the lifetime of the IC and the final electronic application in a multi-stress environment.