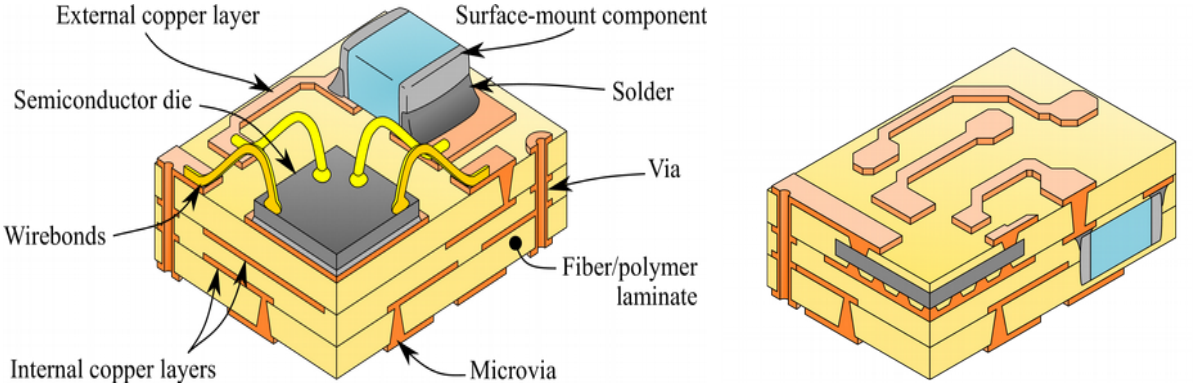
PhD topic

«Highly integrated power building block»

Institution: Laboratoire Ampère, Villeurbanne, France
Supervisor: Mr. Cyril BUTTAY (CNRS, INSA de Lyon)
Email : cyril.buttay@insa-lyon.fr

Background :

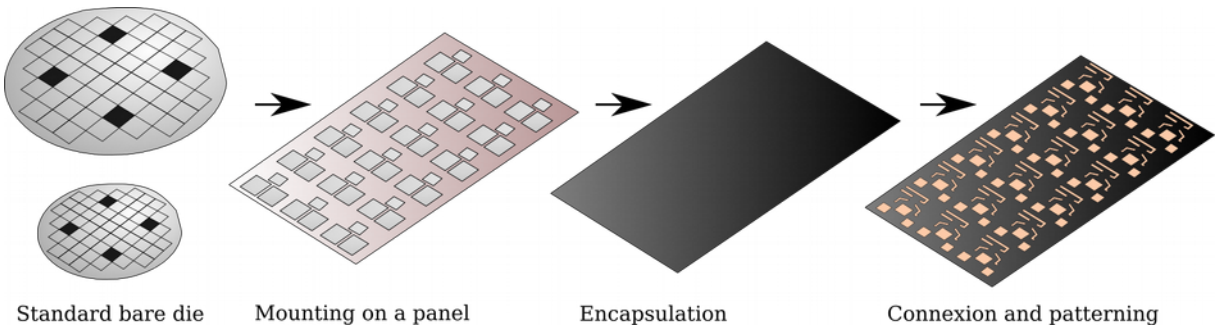


Left : a standard Printed Circuit Board, with surface-mount components. Right : the components are embedded within the substrate, resulting in a more compact system, with improved thermal and electrical performances.

In the recent years, Printed Circuit Board (PCB) embedding has attracted a lot of attention in the field of power electronics. It offers a solution to reduce circuit parasitics (in particular parasitic inductance), and to improve the thermal capability of PCB substrates (by placing heat dissipating elements closer to the cooling areas). In particular, a lot of efforts has been devoted to the semiconductor dies [1]. Embedding of other components (passives, control ICs, etc.) is also interesting. For example, at Ampère, we developed a technology to design and embed large (>50 mm diameter) magnetic devices [2, 3].

Despite the research effort, many hurdles must be overcome for this technology to really become mainstream. In particular, bare semiconductor dies currently require a specific process prior to embedding : the current technologies require a thick (5-10 µm) layer of copper to be applied on the connections of the dies, which is not a standard practice in the industry. Furthermore, the current embedding technologies are not very well suited to variations in the devices thickness (e.g. when embedding several dies with different semiconductor thickness) or to devices with very fine connection pitch.

The objective of this PhD topic is to develop a « pre-packaging » technology. This pre-packaged building-block would host one or several dies, and would provide easy access to their terminals, in a convenient way for PCB embedding. This requires to address thermal, electrical and manufacturing issues. The idea is to take advantage of current developments in the *Fan-Out Wafer-Level Packaging* (FO-WLP) technology which is used in microelectronics to integrate dies with a high interconnect density.



Fan-Out Wafer-Level Packaging principle

Keywords

Printed Circuit Board, Power Electronics integration, Manufacturing Technologies, Electrical, thermal, mechanical modeling

Objectives

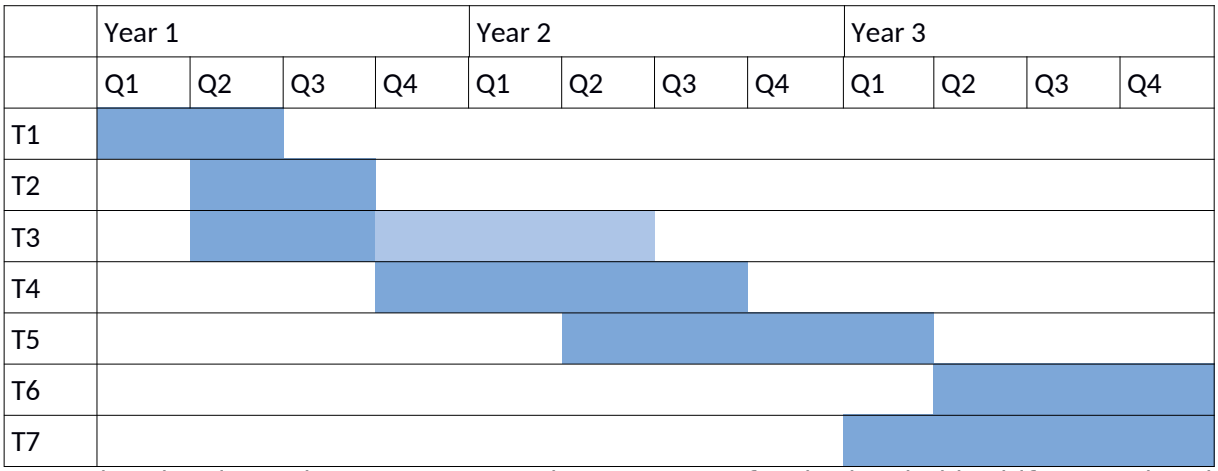
- To define the structure to be integrated as a building block (circuit diagram, components type and count…), to achieve both a satisfying modularity and high performances (high switching speed, low electro-magnetic interference, good thermal management…). This study will be based on modeling software (Comsol, Q3D extractor, Ansys mechanical…)
- To extract compact models of the building block for easy system-level simulation of converters including this brick.
- To develop the FO-WLP technology for power devices. While a number of FO-WLP technologies have been introduced over the years, their compatibility with power semiconductor devices must be verified. In particular, power devices have a backside contact which is not used for microelectronics devices, and they experience much stronger voltage stresses). Existing technologies will therefore be assessed. Should no satisfying technology be found, an in-house technology will be developed based on SU-8 photosensitive thermoset polymer and copper physical vapor deposition, followed by electroplating. In any case (existing technology or in-house developments), the technology will be evaluated through practical demonstrators as well as through thermo-mechanical simulations (to assess the reliability of the building block in conditions of thermal cycling).

Finally, a converter will be built using PCB embedded building blocks.

Tentative planning :

- T1 : Literature review : modelling, FO-WLP (with the objective to generate an evaluation matrix of the technologies), PCB embedding, Requirements of power electronic packaging
- T2 : Acquisition of the modeling and simulation skills, application to converters which are available in the lab
- T3 : Technological developments (the effort on this task will depend on whether suitable FO-WLP technologies have been identified or not)
- T4 : Definition of the “building block”, based on simulations and circuit analysis.

- T5 manufacturing of the building blocks; experimental testing and characterization.
- T6 manufacturing of a converter which embedds the building block(s) in the PCB.
- T7 Memoir writing up.



Note: the planning only covers 36 months to account for the inevitable drifts associated with experimental developments

Scientific challenges

- definition of a building block which offers high performances and yet maintains a sufficient modularity to ensure its use in many converters.
- Definition of the requirements for the materials used in the FO-WLP: coefficient of thermal expansion, operating temperature, processability...
- Identification of the current FO-WLP technologies which meet the requirements of power electronics, or development of specific technological steps.
- Definition of thermal management and electrical insulation techniques which meet the requirements of power electronic devices.
- Physical implementation of a proof of concept

Expected original contributions

Current FO-WLP technologies are dedicated to low power microelectronics applications, with a high number of interconnects. Power electronics, which require much fewer interconnects, but experience high voltage, high current and high power dissipation are not addressed. WO-WLP packages are designed on a chip-per-chip basis, without any regard for modularity.

With this work, we should be able to demonstrate the application of FO-WLP to power electronics, for higher voltage levels (up to 1200 V), and that combiding FO-WLP and PCB embedding makes sense to fully take advantage of the recent developments in power semiconductor technology (wide bandgap materials such as SiC or GaN).

Applicant profile

The applicant should be trained as an engineer in electrical or material sciences, with a clear desire to expand his/her knowledge to other domains. An experience in the micro-fabrication technologies or in electronic design would be appreciated. He/she will work in a team with other students involved in PCB embedding, so good interpersonal skills are expected. A good level of English is mandatory.

Professional development and perspectives

During the PhD, the applicant will develop his/her knowledge in electronic design, manufacturing technologies, as well as his/her experimental skills. With the growing demand worldwide for better power converters (more efficient, more "green"), the skills of the newly trained doctor will be highly looked after, both in academia and industry.

A natural outcome is to join the research and development team in the electronics industry, but the high scientific level of the topic will also allow the applicant to pursue an academic career.

References

[1] Alderman, A.; Burgyan, L.; Narveson, B. & Parker, E. "3-D Embedded Packaging Technology" *IEEE Power Electronics Magazine*, 2015, 30-39

[2] Caillaud, R.; Buttay, C.; Le Lesle, J.; Morel, F.; Mrad, R.; Degrenne, N.; Mollov, S. & Combettes, C. "High power PCB-embedded inductors based on ferrite powder" *5th Micro/Nano-Electronics, packaging and assembling, design and manufacturing forum MiNaPAD 2017*, 2017

[3] Caillaud, R.; Buttay, C.; Mrad, R.; Le Lesle, J.; Morel, F.; Degrenne, N. & Mollov, S. "Comparison of planar and Toroidal PCB integrated inductors for a multi-cellular 3.3 kW PFC" *Integrated Power Packaging (IWIPP), 2017 IEEE International Workshop On*, 2017, 1-5

De Jong, E.; Ferreira, B. & Bauer, P. "Toward the Next Level of PCB Usage in Power Electronic Converters Power Electronics", IEEE Transactions on, 2008, 23, 3151-3163

Marxgut, C.; Muhlethaler, J.; Krismer, F. & Kolar, J. W. "Multiobjective optimization of ultraflat magnetic components with PCB-integrated core" *IEEE Transactions on Power Electronics, IEEE*, 2013, 28, 3591-3602

Randoll, R.; Asef, M.; Wondrak, W.; Böttcher, L. & Schletz, A." Characteristics and aging of PCB embedded power electronics" Microelectronics Reliability, 2015, 55, 1634 – 1639

Brizoux, M.; Grivon, A.; Maia Filho, W.; Monier-Vinard, E.; Stahr, J. & Morianz, M. "Industrial PCB development using embedded passive & active discrete chips focused on process and DfR1 PLUS". Produktion von Leiterplatten und Systemen, 2010, 12, 2670

Hofmann, T.; Gottschling, S.; Wondrak, W. & Randoll, R. "Integration of electronic components into PCB for electromobility application" Electric Drives Production Conference (EDPC), 2012 2nd International, 2012, 1-4