PhD thesis: Building and analyzing processing chains on FPGAs with strong time and hardware constraints

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Context and motivations

Increasing number of projects require real-time processing application in multidisciplinary research context. More and more applications are under strong processing-time and hardware constraints, which led to use FPGAs. Unfortunately, programming FPGAs (in VHDL or Verilog) is still very complex and can be achieved by specialists only. In the recent years, tools (called HLS tools) for transformation of high level languages like C into VHDL are becoming more efficient but are by their very nature limited to applications with low constraints. Another existing tool is Simulink/HDL coder which links functional blocks. This is the simplest way to create, debug and test a processing chain aided by simulation. But the result is rarely applicable directly without a minimum knowledge in FPGAs programing and their internal architecture. There are two limitations of this approach. Firstly, they do not take into account the physical characteristics of the target FPGA. Secondly, they cannot check that an input stream is correctly processed by a chain, apart from creating a lot of benchmarks which is boring and time consuming for the developer. To summarize, these tools neither analyze the evolution of stream structure, nor test if blocks are really able to process the stream taking into account a chosen FPGA. So they are not a solution to problems requiring processing chains with strong processing-time and hardware constraints. A concept of solution to this problem has been proposed in collaboration with the company Armadeus System. It has been developed together with applications in a PhD thesis which completion is expected within few months. It provides a first solution for chains with limited complexity, limited generality and limited access to memories.

Goals

The goal of the present thesis is to improve the theoretical basis of our approach and to extend significantly its range of applicability to more complex and more general parallel chains as well as to allow concurrent access to memory. The contributions will be developed within the LABEX ACTION
and will cover theoretical basis, implementation and proof of concept through applications from FEMTO-ST and supported by the LABEX FIRST-TF. Works can be divided in three main parts.

First, a model of the blocks and their interconnections will be developed. Each functional block is associated with real implementations (developed by VHDL/Verilog experts) that must also be modeled in terms of resources and processing capacities. Based on such a model, a chain can be analyzed to check if data streams are correctly processed by the blocks. The size and structure of the streams are well taken into account as well as their synchronization. If the basic version of the chain does not lead to a correct result, interconnection graph must be modified, for example by inserting delays or FIFOs between particular blocks. Combinatorial optimization algorithms could be used to choose a minimal set of modifications yielding synchronization of parallel streams. Whatever the case, the solution should choose a block implementations resulting in an operational design for a target FPGA, minimizing the resource consumption, the processing time and the latency.

Then, the question of modeling and using an existing block in a chain will be addressed. For this purpose, a characterization method based on series of tests will be developed.

Finally, the above works will be validated in the time-frequency field where the goal is time measurement at extremely high precision using controlled ultra-stable oscillators. In our institute a group is actively transferring analog processing method to digital processing implemented on FPGA. The resulting processing chains are strongly constrained and will be used as examples of applications and tested over different models of FPGAs. Other possible examples could be considered as processing for images or for large arrays of microsystems (e.g. arrays of micro-mirrors or CMUTs).

**Required and optional knowledge**

A good set of knowledge is required in C/C++ programming, graph theory and combinatorial optimization technics. VHDL programming and FPGA architecture knowledge would be an advantage but is not mandatory since it can be acquired during the thesis.